REMARKS

No claims have been amended. Claims 1-22 are pending in the application. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Claims 1-3, 8-12, 14 and 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata in view of Miyazaki. Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyazaki, Yamagata, and Nakajima. Claims 4, 5 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyazaki, Yamagata, and Morita. Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyazaki, Yamagata, and Negishi. Claims 15, 16, 18 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagata in view of Miyazaki and Kane. Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyazaki, Yamagata, Kane and Nakajima. The rejections are respectfully traversed.

Claim 1 recites a display unit for displaying an image, and a drive unit for driving the display unit, the drive unit being connected by a plurality of signal lines. According to claim 1, the "display unit comprises a plurality of display pixels arranged in a matrix form and the signal lines are arranged in each column." Claim 1 further recites that the "drive unit comprises a ladder resistor, impedance converters each having an input connected to an output of the ladder resistor, gray level voltage wires each connected to the output of the impedance converters, gray level voltage selecting means selectively connecting said gray level voltage wires to said plurality of signal lines." According to claim 1, "the number of said impedance converters matches the number of said gray level voltage wires and matches a number of a plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires." As argued previously, Applicants respectfully submit that the cited combinations fail to disclose, teach or suggest the subject matter of claim 1 (as well as the subject matter of claims 2-22).

The Office Action states that Yamagata teaches an image display terminal system with a circuit that "has a ladder resistor and a plurality of gray voltage wires connected to an output of the

ladder resistor (See Fig. 2, lines 6, NLN); group of signal lines are connected to the gray level voltage wires via a gray level voltage selector (See Figs. 1, 2, items 3, NLN, See page 4, paragraphs 0063-0064)..." Office Action at 3-4. Applicants respectfully disagree because Yamagata merely teaches an image display terminal system having a ladder resistor (item 6 in Figure 2), a gray level voltage selector (item 3 in Figure 1) connected to the output of the ladder resistor, the impedance converters (OP in Figure 1) connected to the output of the gray level voltage selector and a plurality of pixel signal wires connected to the output of the impedance converters. As illustrated in a prior response, Yamagata's system looks like the following: gray level voltage wires->impedance converters-> signal lines. This is different than the claimed invention.

The Office Action also states that Miyazaki teaches "impedance converters connected to an output of a ladder resistor (see Fig. 3, items R1-R5) and gray level voltage wires constituting output lines connected to the impedance converters (See Fig. 3, items A1-A5, V1-V5, from Col. 3, Line 58 to Col. 4, Line 2)." Applicants respectfully disagree because Miyazaki merely teaches an image display terminal system having a ladder resistor, the impedance converters connected to the output of the ladder resistor and a plurality of pixel signal wires connected to the output of the impedance converters. As illustrated in a prior response, Miyazaki's system looks like the following: ladder resistor ->impedance converters-> signal lines. This is different than the claimed invention.

Yamagata and Miyazaki are both directed to the connecting relationship having impedance converters connected to the output of the ladder resistor and a plurality of pixel signal wires connected to the output of the impedance converters. As such, Yamagata and Miyazaki necessarily teach the same connecting relationship. The feature of the claimed invention that the number of impedance converters matches the number of gray level voltage wires and matches a number of a plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires cannot be (and is not) taught by any of the cited references, even when considered in combination. Applicants also direct the Examiner's attention to Miyazaki's structure and its number of impedance converters (A1,A2,A3,A4,A5), which matches

the number of pixel matrix wires (V1,V2,V3,V4,V5), which necessarily fails to teach the above features of the claimed invention.

Furthermore, the cited combinations fail to disclose, teach or suggest "an image display apparatus having a drive unit including a ladder resistor, impedance converters each having an input connected to an output of a ladder resistor, gray level voltage wires each connected to the output of the impedance converters, wherein the number of said impedance converters matches the number of said gray level voltage wires, and matches a number of a plurality of gray level voltage selectors connected to the gray level voltage wires in three separate phases when the analog image signal voltages are written onto the signal lines," as is recited in claim 16.

In addition, the cited combinations fail to disclose, teach or suggest a "drive circuit having a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor; said group of signal lines are connected to said gray level voltage wires via a gray level voltage selector; each gray level voltage wire is connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires; at least the display pixels, the group of signal lines, the gray level voltage selector and the gray level voltage wires are provided over the same substrate; and wherein the analog image signal voltages are written in three separate phases when the analog image signal voltages are to be written onto the signal lines," as is recited in claim 19.

Similarly, the cited references do not teach or suggest an image display terminal comprising a "drive circuit [having] a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor; said group of signal lines are connected to the gray level voltage wires via a gray level voltage selector; each of said gray level voltage wires connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires; and at least the display pixels, the group of signal lines, the gray level

voltage selector and the gray level voltage wires are provided over a single substrate," as recited in claim 20.

As such, the primary references fail to disclose, teach or suggest all of the limitations of claims 1, 16, 19 and 20. Applicants respectfully submit, that the other cited references do not cure the deficiencies of Yamagata and Miyazaki. That is, Nakajima is relied upon for disclosing an offset canceling unit, but adds nothing to rectify the above-noted deficiencies. Morita is relied upon for disclosing a differential amplifying circuit using field-effect transistors. Negishi is relied upon for disclosing a ladder resistor configured as one resistor, but adds nothing to rectify the deficiencies of Miyazaki and Yamagata. Kane is relied upon for disclosing three separate phases when the analog image signal voltages are written onto the signal line, but adds nothing to rectify the deficiencies of Yamagata and Miyazaki.

In addition, as previously noted by Applicants, according to the last paragraph of claim 1, it can be seen that one of the features of the claimed invention is that the impedance converters are connected between the ladder resistor and the gray level voltage selecting means (e.g., DA converters). According to the present application, the DA converters 7 may be e.g., the voltage selecting type DA converters 7 that select naturally a gray level voltage by means of the gray level selecting transistors 42, 43, 44 (Figure 2), or any other type. In addition, according to the above structure of the claimed invention and referring also to Figure 3 of the present application, there is another outstanding feature of the claimed invention. As described at page 3, ll. 15-19 of the specification:

> According to these aspects of the invention, analog active circuits such as the impedance converters need not be as many as the number of signal lines but are sufficient in the same number as the gray level voltage wires.

For example, referring to Figure 3 and in accordance with the claimed invention, Applicants submit that it is enough to provide 64 impedance converters for the system of 64 gray voltage levels when using the above connection of: ladder resistor 15→ impedance converters 14→ gray level voltage selecting means. In other words, the number of impedance converters matches

the number of gray level voltage wires and matches a number of the plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires. This is something not found in the prior art.

The above feature of the claimed invention will also solve another problem currently existing in the art. As set forth in the specification at page 1, lines 11-13, "there is a problem that building in as many analog active circuits such as a buffer amplifier as signal lines pulls down the yield." The claimed invention overcomes this problem. The prior art image display apparatus according to Yamagata or Miyazaki, on the other hand, will require providing 1920 (i.e., 640*3) horizontal pixels in the Video Graphics Array because of their connecting relationships in which the impedance converters are connected to the output of the DA converters.

Claims 2-15 and 22 depend from claim 1 and are allowable along with claim 1. Claims 17-18 depend from claim 16 and are allowable along with claim 16. Claim 21 depends from claim 20 and is allowable along with claim 20. Accordingly, the rejections should be withdrawn and the claims allowed.

In view of the above, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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